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### (54) MICROMECHANICAL SWITCH.

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## Description

This invention relates to a method of making a micromechanical switch. In particular, the invention is concerned with the fabrication of micromechanical beams, bridges and torsion elements for use in optical switches and modulators.

Silicon based micromechanical switches, which incorporate micromachined deflecting beams, bridges or torsion elements (switch elements) are known. Typically, this type of device is formed by etching a switch element from monocrystalline silicon, the etching process being such as to form a cavity or well beneath the switch element. Electrodes are then added (or formed in the monocrystalline silicon) for controlling the switch element. When making mirror switches or modulators, the surface of the switch element is provided with a coating of reflective metal. Such switches offer significant advantages compared with conventional switches, these advantages arising from their small size, fast response and negligible ageing effects. Moreover, they can be manufactured by techniques that are compatible with standard integrated circuit (IC) processing methods, and so offer the potential of batch processing and of integration with associated electronic circuitry.

For some optical switching applications, it is advantageous to use larger switch elements than those which can be made by known micromachining techniques (typically 30-75µm). Unfortunately, fabrication problems arise as the size of the switch element is increased. Thus, if the switch element has a dimension greater than 300µm, a very high degree of etching selectivity is required. This is because the region to be protected from etching is coated with an etch-resistant masking layer as thin as 0.1 to 0.2 µm, and the material beneath the switch element (which is to be undercut) must be completely eroded. This calls for a long over-etch, which needs a selectivity of more than 3000:1 between the undercut region and the etch mask. To give some idea of this constraint, Si<sub>3</sub>N<sub>4</sub> is usually used as a protective mask against the usual oxide etchant (buffered HF), but the SiO<sub>2</sub>:Si<sub>3</sub>N<sub>4</sub> etch ratio is only 50:1. Similarly, where an anisotropic Si etchant is used to etch {100} planes quickly, whilst "etch-stopping" on {111} planes, selectivity is typically 50:1 for ethylene diamine pyrocatechol and water (EDP) and between 100:1 and 300:1 for KOH.

Moreover, it is important that the edges of the cavity formed beneath the switch element are well defined during the undercut etching process. Thus, if an undercut of several hundred µm is to be formed (which is necessary for large area switch elements), a lateral etch stop layer is required around the cavity edges to prevent the cavity being enlarged by several hundred µm per side. Since some enlargement is tolerable, a selectivity of greater than 100:1 is adequate here. However, even this degree of etch selectivity is difficult to achieve.

Another problem that can arise with the manufacture of mirror switches/modulators is that the metal reflectivity can be affected by the etching process. In order to overcome this problem, the metal may be passivated (i.e. coated with non-etching material) prior to the deep undercut etch step. This passivating layer must be formed by a low temperature process to avoid thermal damage to the metal film and stress damage to the switch element. Unfortunately, low temperature passivating layers have a poor etch resistance, so it is difficult to prevent the metal reflectivity being affected.

When the switch element of such a switch is controlled electronically, very high voltages may be required, in which case it is important to obtain good isolation/breakdown strength between the control electrodes. If the switch element is a torsion element, this is very difficult to achieve monolithically. Furthermore, it is difficult to prevent the torsion bars of such a torsion element from deflecting under the forces used to control the element.

The aim of the invention is to provide a method of making micromechanical switches which does not suffer from these problems. US-A-4 805 038 discloses an apparatus which includes a kind of micromechanical optical switches formed by an etching method.

The present invention provides a method of making a micromechanical switch, the method comprising the steps of:-

- a) forming a first sacrificial layer on a substrate;
- b) forming a second sacrificial layer as an island on the first sacrificial layer;
- c) forming a switch element layer of resilient material on the second sacrificial layer;
- d) defining the outline of a switch element on the switch element layer;
- e) defining the outline of a window;
- f) etching an aperture in the second sacrificial layer through the window using an etchant which laterally undercuts that portion of the switch element layer which is to form the switch element; and
- g) etching the first sacrificial layer through the aperture in the etched second sacrificial layer to define a cavity beneath said portion.

Advantageously, the first sacrificial layer is an oxide layer formed by deposition or thermal growth, and the second sacrificial layer is a polysilicon layer formed by deposition. Preferably, the second sacrificial layer has a thickness which is small compared with that of the first sacrificial layer. Conveniently, the thickness of

the first sacrificial layer is substantially  $10\mu\text{m}$ , and the thickness of the second sacrificial layer is between  $0.5$  and  $2\mu\text{m}$ .

The method may further comprise the step of forming a nitride layer on the second sacrificial layer prior to the formation of the switch element layer, the nitride layer having a thickness of between  $0.1$  and  $0.4\mu\text{m}$ .

Preferably, the switch element layer is doped polysilicon which is formed by deposition, the thickness of the switch element layer being between  $0.5$  and  $2\mu\text{m}$ .

Advantageously, the outline of the switch element is defined photolithographically, and the switch element is formed by etching the switch element layer selectively to the nitride layer. Conveniently, the switch element layer is etched using a plasma etch.

A further nitride layer may be deposited following the step of etching the switch element layer, the further nitride layer having a thickness of between  $0.1$  and  $0.3\mu\text{m}$ . The method may further comprise the step of forming a layer of metal on that portion of the further nitride layer which covers the switch element. The method may further comprise the step of forming a passivating layer over the layer of metal.

The outline of the window may be formed photolithographically on the passivating layer. Preferably, the passivating layer is etched, through the window, using a buffered HF etchant. Both nitride layers may then be etched, using the etched passivating layer as a mask, using orthophosphoric acid as the etchant. Alternatively, the passivating layer and both the nitride layers are etched, through the window, by a single plasma etching step. Advantageously, the plasma etching step uses  $\text{CHF}_3$  as the etchant.

The invention may further comprise the step of forming a further layer of metal over part of the passivating layer and part of the first sacrificial layer, the further layer of metal being formed prior to etching the passivating layer. Preferably, the further layer of material is formed by electroplating and has a thickness of between  $3$  and  $4\mu\text{m}$ .

Advantageously, the second sacrificial layer is etched using EDP as the etchant, and the first sacrificial layer is etched using a buffered HF etchant.

The method may further comprise the step of forming one or more electrodes in the substrate prior to the formation of the first sacrificial layer.

The invention also provides a micromechanical switch directly obtained by the method described above (cf. Article 64(2), EPC).

The invention will now be described in greater detail, by way of example, with reference to the accompanying drawings, in which:-

- Fig 1 to 3 are schematic longitudinal cross-sections which illustrate the basic process sequence of the fabrication method of the invention;
- Fig 4 to 6 are diagrammatic longitudinal cross-sections through a practical device constructed in accordance with the invention at various stages of fabrication;
- Fig 7 is a diagrammatic plan view of the device at an intermediate stage of fabrication;
- Fig 8 is a diagrammatic transverse cross-section through the finished version of a device which is a modified version of the device of Figs 1 to 4;
- Fig 9 is a diagrammatic cross-section, similar to that of Fig 1, of a modified form of device; and
- Fig 10 to 12 are diagrammatic longitudinal cross-sections through an electrical switch device constructed in accordance with the invention at various stages of fabrication.

Referring to the drawings, Fig. 1 shows an intermediate stage in the basic process for fabricating a micromechanical switch. A first relatively-thick sacrificial layer S1 is formed on a silicon substrate S, the substrate containing one or more lower electrodes (not shown). A second, relatively-thin sacrificial layer S2 is then formed on the first sacrificial layer S1. A cantilever beam layer S3 is then formed on the layer S2. This stage of the process is shown in Fig. 1. The layer S2 is then removed (using a suitable etchant) from beneath that portion of the layer S3 which is to form a cantilever beam B by a long undercut (see Fig. 2). A cavity C is then etched in the layer S1 through the cavity formed in the layer S2. The deep cavity C is, therefore, etched in a time related to the thickness of the layer S1, rather than to the depth of undercut. The requirements for very high etch-rate selectivity and very thick layers are, thus, separated into two different materials.

Figs 4 to 6 show various stages of the fabrication process of a practical device. Thus, Fig. 4 shows an intermediate stage in the fabrication process of an optical micromechanical switch. The starting point for the process according to the invention is a monocrystalline silicon substrate 1. A lower electrode 2 is formed in the substrate 1 by a diffusion process in which a heavily-doped region defines the lower electrode. The heavily-doped region may be  $p^+$  (in which case boron is used as the dopant) or  $n^+$  (in which case arsenic or phosphorus is used as the dopant).

A thick ( $\sim 10\mu\text{m}$ ) sacrificial oxide layer 3 is thermally grown on the substrate 1, after which a thin ( $0.5$  to  $2.0\mu\text{m}$ ) sacrificial polysilicon layer 4 is deposited by a chemical vapour deposition (CVD) process. Using a photolithographic technique, the outline of a cavity (to be described below) is then printed onto the thin sacrificial

layer 4 (see Fig. 7). The outline of the cavity is then defined by etching the polysilicon layer 4 using a plasma etching or a wet etching process. The layer 4 is then covered with a protective nitride layer 6, this layer being deposited by a CVD process - either plasma enhanced CVD (PECVD) or low pressure CVD (LPCVD) - to a depth of 0.1 to 0.4  $\mu\text{m}$ . The layer 6 acts to protect the underside of a layer 7 which is subsequently added.

The layer 7 is a doped polysilicon layer which is deposited by CVD to a depth of 0.5 to 2.0  $\mu\text{m}$ . The layer 7 is doped either p<sup>+</sup> or n<sup>+</sup>, so that this layer can act as an electrode (as described below). The doping of the layer 7 also anneals the polysilicon, thereby relieving stress in this layer. The pattern of a cantilever beam 8 (see Fig. 7) is then printed on the layer 7 by a photolithographic process, and the polysilicon is etched away using a plasma etch to define the shape of the beam. The plasma etch is a selective etch which terminates at the nitride layer 6.

A second nitride layer 9 is then deposited conformally by CVD, this layer having a thickness of 0.1 to 0.3  $\mu\text{m}$  and acting to protect the top and sides of the beam 8. The conformal deposition of this layer 9 is necessary to ensure adequate protection for the sides of the beam 8. A thin layer 10 of aluminium is then deposited over the layer 9 by evaporation or sputtering. This layer 10 is to constitute both an upper electrode and a mirror surface. The layer 10 must be a thin layer (50 nm to 0.2  $\mu\text{m}$ ) to reduce the stress on the beam 8 which is to be formed out of the polysilicon layer 7. However, a minimum thickness of 0.5  $\mu\text{m}$  of metal is needed in those regions where contact wires for the upper electrode are to be bonded to the layer 10. In practice, therefore, a thick (0.5  $\mu\text{m}$ ) layer of aluminium is deposited over the entire area of the device, and aluminium is subsequently removed by plasma etching, following a photolithographic printing step, everywhere except those contact regions and any necessary wiring tracks. A passivating layer 11, which acts to protect the layer 10 from subsequent processing steps, is then deposited. This layer 11 is a 0.5  $\mu\text{m}$  conformal, low temperature oxide coating which is formed by PECVD. Fig. 4 illustrates the device at this stage of the fabrication process.

The outline 12 (see Fig. 7) of an etch window, which is to open up a cavity 13 (to be described below) whilst protecting the cantilever beam 8, is then formed by a photolithographic technique on the passivating layer 11. The passivating layer 11 is then etched away within the outline 12 using a buffered HF etchant. The nitride layers 6 and 9 are subsequently etched, within the outline 12, using the passivating layer as a mask and orthophosphoric acid as the etchant. The thin sacrificial layer 4 is then etched using EDP as the etchant. This etching step undercuts the polysilicon of the layer 4 beneath the cantilever beam 8. It should be noted that, in EDP, the etching selectivity of polysilicon to nitride is > 6000:1, and the etching selectivity of polysilicon to passivating oxide is > 2500:1. Fig. 2 illustrates the device at this stage of the fabrication process.

The cavity 13 is then formed by etching the thick sacrificial layer 3 using buffered HF. This etching step also strips away the passivating layer 11. In buffered HF, the etching selectivity of oxide to nitride is > 50:1. The etching time is virtually independent of the area of the cavity 13, depending only on the thickness of the layer 3, because the etchant can immediately penetrate fully under the cantilever beam 8. The sidewalls of cavity 13 are undercut by a distance approximately equal to the depth of the cavity.

If a switch having a torsion element is required, the fabrication process described above with reference to Figs 4 to 7 could be modified. Thus, in order to define a torsion element rather than a cantilever beam, the outline of the etch window would be modified to define a pair of torsion bars 14 (see Fig. 8) extending transversely, in opposite directions, from the central region of the torsion element 8'. Moreover, an additional nitride layer 15 would be formed (between the steps, forming the two sacrificial layers 3 and 4) beneath the regions in which the torsion bars 14 are to be formed. In this region, only the thin sacrificial layer 4 is removed in the etching steps which forms the cavity 13, and the resultant pillar (see Fig. 8) forms a support for the torsion element 8', thereby minimising bending of the element.

Fig. 9 shows an intermediate stage (equivalent to Fig. 4) in the fabrication of another form of modified device, which incorporates a cantilever beam 8". The beam 8" is a multi-layer beam which incorporates a piezoelectric layer 16. The beam 8" thus constitutes a piezoelectric bimorph actuator, the deflection of which is controlled by the electric field within the piezoelectric layer 16.

Figs 10 to 12 show how the fabrication process of the invention can be modified to make an electric micromechanical switch. As most of the process steps are similar to those of the process described above with reference to Figs. 4 to 8, only the modified steps of the process of Figs. 10 to 12 will be described in detail and similar reference numerals (with the addition of 100) will be used for similar parts. Thus, a lower electrode 102 is deposited (for example by sputtering a refractory metal) on a monocrystalline silicon substrate 101. Thick and thin sacrificial layers 103 and 104 respectively are then formed, after which a switch element layer 107 is formed. This layer 107 is a conducting layer, which is to form a cantilever beam switch element 108 (see Fig. 12), made for example of doped polysilicon or metal. This layer could also be an insulating layer coated top and bottom with metal. A third sacrificial (oxide) layer 111 is deposited by PECVD, this layer acting as a passivating layer and having a thickness of between 1 and 2  $\mu\text{m}$ . A 3 to 4  $\mu\text{m}$  thick metal layer 120 is then formed, by electroplating, over part of the layer 111 and over part of the layer 103. This stage of the process is shown

in Fig. 10.

The sacrificial layer 111 is then etched out using a buffered HF etchant to leave a gap between the layer 107 and the layer 120 (see Fig. 11). The remaining steps of the process are similar to the final process steps described above with reference to Figs 4 to 6, and relate to the formation of the beam 108 and the cavity 113. Fig. 12 shows the finished electric micromechanical switch, in which the beam 108 curves naturally upwards so as to make electrical contact with the layer 120. This curve is formed as a result of an upward bending movement imparted to the beam 108 due to intrinsic stresses formed in the beam by the use of two different materials. The beam 108 can then be controlled electrostatically, using the lower electrode 102, to make or break electrical contact between the beam and the layer 120, thus forming a one-way switch. A two-way switch could be formed by providing a further electrode within the cavity 113. Alternatively, the beam 108 would be a piezoelectric bimorph element, which could be bent both upwardly and downwardly to make contact with the lower electrode 102 and the layer 120 (upper electrode).

The micromechanical switch fabrication process described above has the following advantages:-

1. It offers complete flexibility in the placement of electrodes on the base of the cavity and on the switch element, so it is adaptable to torsion elements and bridges, as well as cantilever beams.
2. It allows the enlargement of the cavity 13 to be easily controlled compared with methods using a single sacrificial layer (which requires a very deep etch which would give problems with later step coverage).
3. It does not require an epitaxial growth step.
4. The required etch selectivities can all be achieved with materials which are readily available.
5. It could be used for both normally-open and normally-closed electrical switches.
6. It intrinsically gives a multi-layer cantilever allowing stressed to be compensated.

It will be apparent that the fabrication process described above could be modified in a number of ways. For example, the lower electrode could be formed by the deposition of a refractory metal or by ion implantation.

Where a single lower electrode 2 is required, the entire substrate 1 could be doped (either n<sup>+</sup> or p<sup>+</sup>). It would also be possible, for example where a torsion element constitutes the switching element, to provide a pair of lower electrodes. It would also be possible to deposit the thick sacrificial oxide layer 3 by, for example, PECVD, particularly if a metal electrode 2 is utilised. Instead of forming the beam 8 (switch element) from a polysilicon layer 7, this layer would be SiO<sub>2</sub> deposited by, for example, PECVD. Moreover, the metal used for the electrode/mirror 10 would be gold instead of aluminium. In this case, there would be no need for the subsequent formation of the passivating layer 11. Where a passivating layer 11 is necessary, this could alternatively be a nitride layer. As an alternative to using two etching steps to etch the passivating layer 11 and the two nitride layers 6 and 9, these layers would be etched in a single plasma etching step using, for example, CHF<sub>3</sub>.

## Claims

1. A method of making a micromechanical switch, the method comprising the steps of:-
  - a) forming a first sacrificial layer (S<sub>1</sub>, 3, 103) on a substrate (S, 1, 101);
  - b) forming a second sacrificial layer (S<sub>2</sub>, 4, 104) as an island on the first sacrificial layer;
  - c) forming a switch element layer (S<sub>3</sub>, 7, 107) of resilient material on the second sacrificial layer;
  - d) defining the outline (8, 8') of a switch element on the switch element layer;
  - e) defining the outline (12) of a window;
  - f) etching an aperture in the second sacrificial layer (S<sub>2</sub>, 4, 104) through the window using an etchant which laterally undercuts that portion of the switch element layer which is to form the switch element; and
  - g) etching the first sacrificial layer (S<sub>1</sub>, 3, 103) through the aperture in the etched second sacrificial layer to define a cavity beneath said portion.
2. A method as claimed in claim 1, wherein the first sacrificial layer (3, 103) is an oxide layer formed by deposition or thermal growth.
3. A method as claimed in claim 1 or claim 2, wherein the second sacrificial layer (4, 104) is a polysilicon layer formed by deposition.
4. A method as claimed in any one of claims 1 to 3, wherein the second sacrificial layer (4, 104) has a thickness which is small compared with that of the first sacrificial layer (3, 103).
5. A method as claimed in claim 4, wherein the thickness of the first sacrificial layer (3, 103) is substantially

10µm, and the thickness of the second sacrificial layer (4, 104) is between 0.5 and 2µm.

6. A method as claimed in any one of claims 1 to 5, further comprising the step of forming a nitride layer (6) on the second sacrificial layer prior to the formation of the switch element layer.
7. A method as claimed in claim 6, wherein the nitride layer (6) has a thickness of between 0.1 and 0.4µm.
8. A method as claimed in any one of claims 1 to 7, wherein the switch element layer (7, 107) is doped polysilicon which is formed by deposition.
9. A method as claimed in claim 8, wherein the thickness of the switch element layer (7, 107) is between 0.5 and 2µm.
10. A method as claimed in any one of claims 1 to 9, wherein the outline of the switch element (7, 107) is defined photolithographically.
11. A method as claimed in claim 6, or in any one of claims 7 to 10 when appendent to claim 6, wherein the switch element (7, 107) is formed by etching the switch element layer selectively to the nitride layer (6).
12. A method as claimed in claim 11, wherein the switch element layer (7, 107) is etched using a plasma etch.
13. A method as claimed in claim 11 or claim 12, wherein a further nitride layer (9) is deposited following the step of etching the switch element layer (7, 107).
14. A method as claimed in claim 13, wherein the further nitride layer (9) has a thickness of between 0.1 and 0.3µm.
15. A method as claimed in claim 13 or claim 14, further comprising the step of forming a layer of metal (10) on that portion of the further nitride layer (9) which covers the switch element (7, 107).
16. A method as claimed in claim 15, further comprising the step of forming a passivating layer (11) over the layer of metal (10).
17. A method as claimed in any one of claims 1 to 16, wherein the outline (12) of the window is formed photolithographically on the passivating layer (11).
18. A method as claimed in claim 17, wherein the passivating layer (11) is etched, through the window, using a buffered HF etchant.
19. A method as claimed in claim 18, wherein both nitride layers (6, 9) are etched, using the etched passivating layer (11) as a mask, using orthophosphoric acid as the etchant.
20. A method as claimed in claim 17, wherein the passivating layer (11) and both the nitride layers (6, 9) are etched, through the window, by a single plasma etching step.
21. A method as claimed in claim 20, wherein the plasma etching step uses  $\text{CHF}_3$  as the etchant.
22. A method as claimed in any one of claims 18 to 21, further comprising the step of forming a further layer of metal (120) over part of the passivating layer (111) and part of the first sacrificial layer (103), the further layer of metal being formed prior to etching the passivating layer.
23. A method as claimed in claim 22, wherein the further layer of metal (120) is formed by electroplating and has a thickness of between 3 and 4µm.
24. A method as claimed in any one of claims 1 to 23, wherein the second sacrificial layer (4, 104) is etched using EDP as the etchant.
25. A method as claimed in any one of claims 1 to 24, wherein the first sacrificial layer (3, 103) is etched using a buffered HF etchant.
26. A method as claimed in any one of claims 1 to 25, further comprising the step of forming one or more

electrodes (2, 102) in the substrate prior to the formation of the first sacrificial layer.

# Patentansprüche

1. Verfahren zur Herstellung eines mikromechanischen Schalters mit den Schritten:
  - a) Bilden einer ersten Opferschicht (S1, 3, 103) auf einem Substrat (S, 1, 101);
  - b) Bilden einer zweiten Opferschicht (S2, 4, 104) als Insel auf der ersten Opferschicht;
  - c) Bilden einer Schaltelementschicht (S3, 7, 107) aus nachgiebigem Material auf der zweiten Opferschicht;
  - d) Festlegen des Umrisses (8, 8') eines Schaltelements auf der Schaltelementschicht;
  - e) Festlegen des Umrisses (12) eines Fensters;
  - f) Ätzen einer Öffnung in die zweite Opferschicht (S2, 4, 104) durch das Fenster und Verwendung eines Ätzmittels, das den Bereich der Schaltelementschicht, die das Schaltelement formen soll, seitlich unterschneidet; und
  - g) Ätzen der ersten Opferschicht (S, 3, 103) durch die Öffnung in der geätzten zweiten Opferschicht, um unter dem genannten Bereich einen Hohlraum zu erzeugen.
2. Verfahren nach Anspruch 1, bei dem die erste Opferschicht (3, 103) eine Oxidschicht ist, die durch Ablagerung oder durch thermisches Aufwachsen gebildet wird.
3. Verfahren nach Anspruch 1 oder 2, bei dem die zweite Opferschicht (4, 104) eine Polysiliciumschicht ist, die durch Ablagerung gebildet wird.
4. Verfahren nach einem der Ansprüche 1 bis 3, bei dem die zweite Opferschicht (4, 104) eine Dicke hat, die klein ist im Vergleich zu derjenigen der ersten Opferschicht (3, 103).
5. Verfahren nach Anspruch 4, bei dem die Dicke der ersten Opferschicht (3, 103) in etwa 10 µm beträgt und die Dicke der zweiten Opferschicht (4, 104) zwischen 0,5 und 2 µm liegt.
6. Verfahren nach einem der Ansprüche 1 bis 5, mit dem weiteren Schritt des Bildens einer Nitridschicht (6) auf der zweiten Opferschicht vor dem Bilden der Schaltelementschicht.
7. Verfahren nach Anspruch 6, bei dem die Nitridschicht (6) eine Dicke zwischen 0,1 und 0,4 µm hat.
8. Verfahren nach einem der Ansprüche 1 bis 7, bei dem die Schaltelementschicht (7, 107) dotiertes Polysilicium ist und durch Ablagerung gebildet wird.
9. Verfahren nach Anspruch 8, bei dem die Dicke der Schaltelementschicht (7, 107) zwischen 0,5 und 2 µm liegt.
10. Verfahren nach einem der Ansprüche 1 bis 9, bei dem der Umriss des Schaltelements (7, 107) photolithographisch bestimmt wird.
11. Verfahren nach Anspruch 6 oder einem der Ansprüche 7 bis 10, soweit sie sich auf Anspruch 6 zurückbeziehen, bei dem das Schaltelement (7, 107) durch wahlweises Ätzen der Schaltelementschicht bis zur Nitridschicht (6) gebildet wird.
12. Verfahren nach Anspruch 11, bei dem die Schaltelementschicht (7, 107) unter Verwendung von Plasmaätzen geätzt wird.
13. Verfahren nach Anspruch 11 oder 12, bei dem auf den Schritt des Ätzens der Schaltelementschicht (7, 107) hin eine weitere Nitridschicht (9) abgelagert wird.
14. Verfahren nach Anspruch 13, bei dem die weitere Nitridschicht (9) eine Dicke zwischen 0,1 und 0,3 µm hat.
15. Verfahren nach Anspruch 13 oder 14, mit dem weiteren Schritt des Bildens einer Metallschicht (10) auf demjenigen Bereich der weiteren Nitridschicht (9), der das Schaltelement (7, 107) bedeckt.

16. Verfahren nach Anspruch 15, mit dem weiteren Schritt des Bildens einer passivierenden Schicht (11) über der Metallschicht (10).
17. Verfahren nach einem der Ansprüche 1 bis 16, bei dem der Umriss (12) des Fensters photolithographisch auf der passivierenden Schicht (11) gebildet wird.
18. Verfahren nach Anspruch 17, bei dem die passivierende Schicht (11) durch das Fenster unter Verwendung eines gepufferten HF-Ätzmittels geätzt wird.
19. Verfahren nach Anspruch 18, bei dem beide Nitridschichten (6, 9) geätzt werden, indem die geätzte passivierende Schicht (11) als Maske verwendet wird, und wobei Orthophosphorsäure als Ätzmittel verwendet wird.
20. Verfahren nach Anspruch 17, bei dem die passivierende Schicht (11) und beide Nitridschichten (6, 9) durch das Fenster hindurch durch einen einzigen Plasmaätzschritt geätzt werden.
21. Verfahren nach Anspruch 20, bei dem im Plasmaätzschritt  $\text{CHF}_3$  als Ätzmittel verwendet wird.
22. Verfahren nach einem der Ansprüche 18 bis 21, mit dem weiteren Schritt des Bildens einer weiteren Metallschicht (120) über einem Teil der passivierenden Schicht (111) und einem Teil der ersten Opferschicht (103), wobei die weitere Metallschicht vor dem Ätzen der passivierenden Schicht gebildet wird.
23. Verfahren nach Anspruch 22, bei dem die weitere Metallschicht (120) durch Galvanisierung gebildet wird und eine Dicke zwischen 3 und 4  $\mu\text{m}$  hat.
24. Verfahren nach einem der Ansprüche 1 bis 23, bei dem die zweite Opferschicht (4, 104) unter Verwendung von EDP als Ätzmittel geätzt wird.
25. Verfahren nach einem der Ansprüche 1 bis 24, bei dem die erste Opferschicht (3, 103) unter Verwendung eines gepufferten HF-Ätzmittels geätzt wird.
26. Verfahren nach einem der Ansprüche 1 bis 25, mit dem weiteren Schritt des Bildens einer oder mehrerer Elektroden (2, 102) auf dem Substrat, bevor die erste Opferschicht gebildet wird.

#### Revendications

1. Procédé de fabrication d'un commutateur micromécanique, le procédé comprenant les étapes de:
  - a) formation d'une première couche sacrificielle (S1, 3, 103) sur un substrat (S, 1, 101);
  - b) formation d'une seconde couche sacrificielle (S2, 4, 104) sous forme d'un flot sur la première couche sacrificielle;
  - c) formation d'une couche d'élément commutateur (S3, 7, 107) de matière résiliante sur la seconde couche sacrificielle;
  - d) définition du contour (8, 8') d'un élément commutateur sur la couche d'élément commutateur;
  - e) définition du contour (12) d'une fenêtre;
  - f) formation d'une ouverture par attaque chimique dans la seconde couche sacrificielle (S2, 4, 104) par la fenêtre en utilisant un réactif d'attaque qui attaque latéralement cette partie de la couche d'élément commutateur qui doit former l'élément commutateur; et
  - g) attaque de la première couche sacrificielle (S1, 3, 103) par l'ouverture dans la seconde couche sacrificielle attaquée pour définir une cavité en dessous ladite partie.
2. Procédé selon la revendication 1, caractérisé en ce que la première couche sacrificielle (3, 103) est une couche d'oxyde formée par déposition ou tirage thermique.
3. Procédé selon la revendication 1 ou la revendication 2, caractérisé en ce que la seconde couche sacrificielle (4, 104) est une couche de polysilicium formée par déposition.
4. Procédé selon une quelconque des revendications 1 à 3, caractérisé en ce que la seconde couche sacrificielle (4, 104) a une épaisseur qui est petite en comparaison avec celle de la première couche sacrificielle (3, 103).

5. Procédé selon la revendication 4, caractérisé en ce que l'épaisseur de la première couche sacrificielle (3, 103) est sensiblement de 10  $\mu\text{m}$  et l'épaisseur de la seconde couche sacrificielle (4, 104) est entre 0,5 et 2  $\mu\text{m}$ .
6. Procédé selon une quelconque des revendications 1 à 5, comprenant en outre l'étape de formation d'une couche (6) de nitrure sur la seconde couche sacrificielle avant la formation de la couche d'élément commutateur.
7. Procédé selon la revendication 6, caractérisé en ce que la couche de nitrure a une épaisseur entre 0,1 et 0,4  $\mu\text{m}$ .
8. Procédé selon une quelconque des revendications 1 à 7, caractérisé en ce que la couche d'élément commutateur (7, 107) est du polysilicium dopé qui est formé par déposition.
9. Procédé selon la revendication 8, caractérisé en ce que l'épaisseur de la couche (7, 107) d'élément commutateur est entre 0,5 et 2  $\mu\text{m}$ .
10. Procédé selon une quelconque des revendications 1 à 9, caractérisé en ce que le contour de l'élément commutateur (7, 107) est défini par photolithographie.
11. Procédé selon la revendication 6, ou une quelconque des revendications 7 à 10 lorsqu'elle est reliée à la revendication 6, caractérisé en ce que l'élément commutateur (7, 107) est formé par attaque chimique de la couche d'élément commutateur sélectivement jusqu'à la couche (6) de nitrure.
12. Procédé selon la revendication 11, caractérisé en ce que la couche (7, 107) d'élément commutateur est attaquée en utilisant une attaque par plasma.
13. Procédé selon la revendication 11 ou 12, caractérisé en ce que une couche supplémentaire (9) de nitrure est déposée à la suite de l'étape d'attaque chimique de la couche (7, 107) d'élément commutateur.
14. Procédé selon la revendication 13, caractérisé en ce que la couche supplémentaire (9) de nitrure a une épaisseur entre 0,1 et 0,3  $\mu\text{m}$ .
15. Procédé selon la revendication 13 ou la revendication 14, comprenant en outre l'étape de formation d'une couche de métal (10) sur cette partie de la couche supplémentaire (9) de nitrure qui recouvre l'élément commutateur (7, 107).
16. Procédé selon la revendication 15, comprenant en outre l'étape de formation d'une couche (11) de passivation sur la couche de métal (10).
17. Procédé selon une quelconque des revendications 1 à 16, caractérisé en ce que le contour (12) de la fenêtre est formé par photolithographie sur la couche (11) de passivation.
18. Procédé selon la revendication 17, caractérisé en ce que la couche (11) de passivation est attaquée chimiquement, par la fenêtre, en utilisant un réactif d'attaque au HF tamponné.
19. Procédé selon la revendication 18, caractérisé en ce que les deux couches (6, 9) de nitrure sont attaquées chimiquement, en utilisant la couche (11) de passivation attaquée chimiquement comme masque, en utilisant l'acide orthophosphorique comme réactif d'attaque.
20. Procédé selon la revendication 17, caractérisé en ce que la couche (11) de passivation et les deux couches (6, 9) de nitrure sont attaquées, par la fenêtre, par une seule étape d'attaque par plasma.
21. Procédé selon la revendication 20, caractérisé en ce que l'étape d'attaque par plasma utilise le  $\text{CHF}_3$  comme réactif d'attaque.
22. Procédé selon une quelconque des revendications 18 à 21, comprenant en outre l'étape de formation d'une couche supplémentaire de métal (120) sur une partie de la couche (111) de passivation et une partie de la première couche sacrificielle (103), la couche supplémentaire de métal étant formée avant l'attaque de la couche de passivation.

23. Procédé selon la revendication 22, caractérisé en ce que la couche supplémentaire de métal (120) est formée par électrodéposition et a une épaisseur entre 3 et 4  $\mu\text{m}$ .
24. Procédé selon une quelconque des revendications 1 à 23, caractérisé en ce que la seconde couche sacrificielle (4, 104) est attaquée en utilisant l'EDP comme réactif d'attaque.
25. Procédé selon une quelconque des revendications 1 à 24, caractérisé en ce que la première couche sacrificielle (3, 103) est attaquée en utilisant un réactif d'attaque au HF tamponné.
26. Procédé selon une quelconque des revendications 1 à 25, comprenant en outre l'étape de formation d'une ou plusieurs électrodes (2, 102) dans le substrat avant la formation de la première couche sacrificielle.

Fig. 1.

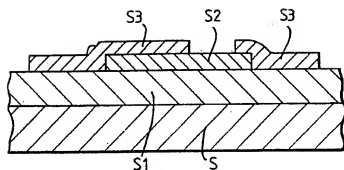


Fig. 2.

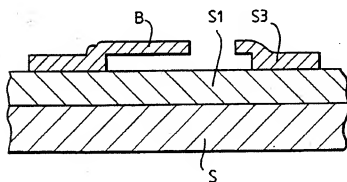


Fig. 3.

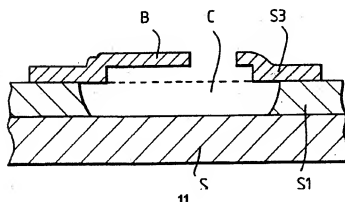


Fig. 4.

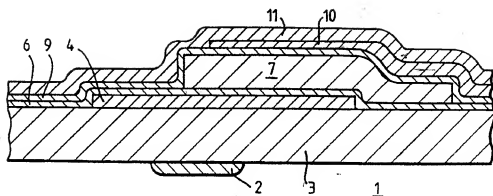


Fig. 5.

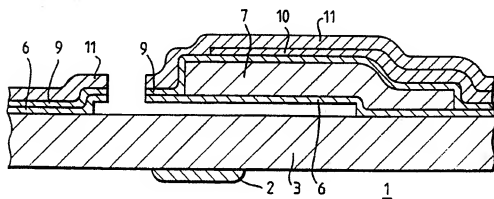


Fig. 6.

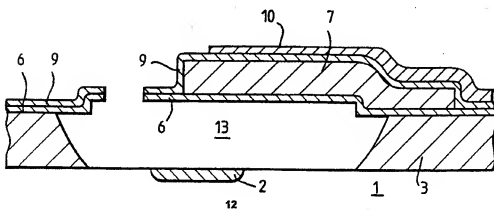


Fig. 7.

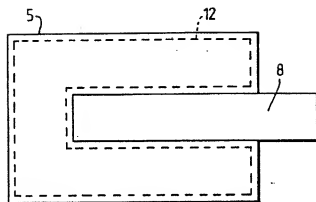


Fig. 8.

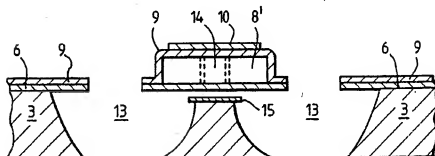


Fig. 9.

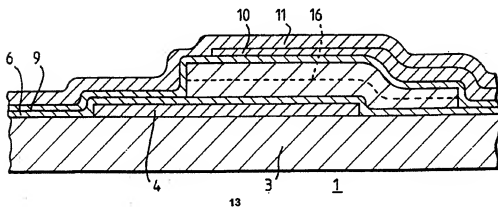


Fig.10.

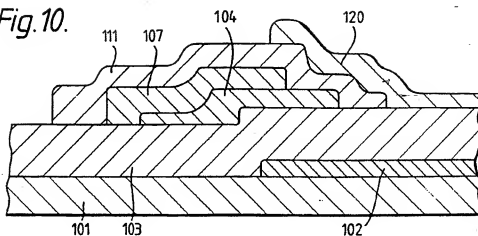


Fig.11.

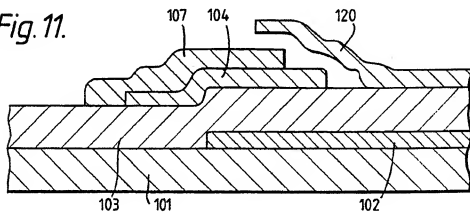


Fig.12.

